WHAT IS CLAIMED IS:

1   1.   Apparatus comprising:

2   a cache including cache lines each of which is configured

3   to store data; and

4   an eviction mechanism configured to evict data stored in

5   one of the cache lines based on validity state information

6   associated with the data stored in the one cache line.

1   2.   The apparatus of claim 1 in which each of the cache lines

2   is configured to store data that corresponds to consecutive

3   addresses in a main memory.

1   3.   The apparatus of claim 1 in which each cache line has

2   multiple portions.

1   4.   The apparatus of claim 3 further comprising a storage for

2   storing validity bits that track the validity of respective

3   portions of the cache line.

1   5.   The apparatus of claim 4 in which the validity bits are

2   set to a predefined value to indicate that the respective

3   portion has been written in full in one write transaction.

1   6.   The apparatus of claim 5 in which the eviction mechanism

2   is configured to evict the cache line when the validity bits

3   all have the predefined value.

1   7.   The apparatus of claim 1 in which the eviction mechanism

2   is configured to evict the data even if the cache is not full

3   and data in other cache lines is not being evicted at the same

4   time.

1   8.   The apparatus of claim 1, further comprising a memory for

2   storing the data evicted by the eviction mechanism.

1   9.   The apparatus of claim 8, further comprising an

2   input/output device that generates the data stored in the

3   cache.

1   10.   Apparatus comprising:

2   cache lines, each configured to store bytes of data that

3   correspond to consecutive addresses in a main memory, each

4   cache line corresponding to a group of validity bits, each of

5   the validity bits tracking a portion of the cache line and

6   being set to a predefined value when the tracked portion of

7   the cache line is fully written in one write transaction; and

8   an eviction component configured to evict the bytes of

9   data stored in one of the cache lines when the group of

10   validity bits corresponding to the cache line are all set to

11   the predefined value.

1   11.   The apparatus of claim 10 in which cache lines are

2   disposed within a write cache memory of a computer chipset.

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1   12.   The apparatus of claim 11 in which the cache lines are

2   compatible with a cache coherent protocol.

1   13.   A method comprising:

2   receiving write transactions associated with data to be

3   written;

4   storing the data into portions of a single cache line of

5   a cache, and

6   evicting the data from the cache line when the cache line

7   is full of data according to stored validity information.

1   14.   The method of claim 13, further comprising writing the

2   evicted bytes of data to a main memory.

1   15.   The method of claim 13, further comprising setting

2   validity bits to a predefined value when respective portions

3   of the cache line is written in full.

1   16.   The method of claim 13 in which the write transactions

2   are sent from an input/output device.

1   17.   The method of claim 16 in which each of the write

2   transactions sent from the input/output device writes a first

3   number of data bytes to one of the cache lines, and the

4   eviction component evicts a second number of data bytes in one

5   eviction operation, the first number being less than the

6   second number.

1   18.   Apparatus comprising:

2   a computer chipset having a cache memory configured to

3   store write data sent from an input/output device and a

4   mechanism configured to evict the write data from the cache

5   memory when a set of predefined conditions are met.

1   19.   The apparatus of claim 18 in which the cache memory also

2   stores additional write data sent from an additional

3   input/output device, and the mechanism also configured to

4   evict the additional write data from the cache memory when the

5   set of predefined conditions are met.

1   20.   The apparatus of claim 18 in which the cache memory is

2   compatible with a cache coherent protocol.

1   21.   The apparatus of claim 18 in which the input/output

2   device initiates write transactions to send the write data,

3   and the mechanism is configured to combine the write data so

4   that the number of eviction operations performed to evict the

5   write data from the cache memory is less than the number of

6   write transactions initiated by the input/output device.

1   22.   A method comprising:

2   initiating write transactions by an input/output device

3 to write data;

4   writing the data into a cache memory;

5   evicting the data from the cache memory; and

6   writing the data into a main memory.

1 23.   The method of claim 22 in which the cache memory contains

2 cache lines configured to store data, each cache line

3 corresponding to consecutive addresses in main memory.

1 24.   The method of claim 23 in which each cache line has

2 multiple portions, each portion corresponding to a validity

3 bit that tracks the status of the corresponding portion.

1 25.   The method of claim 24 in which the validity bit is set

2 to a predetermined value responsive of the number of bytes of

3 data written into the corresponding portion.

1 26.   The method of claim 25 in which the evicting the data

2 from the cache memory comprises evicting the data when the

3 validity bits corresponding to a cache line are all set to a

4 predefined value.